What is claimed is:

CLAIMS

1. A receiver for use in a communications system that employs digitally modulated signals operating in a band of frequencies that is divided into two or more non-overlapping channels comprising:

   an input for receiving a data stream representative of the entire band, with each channel within the band converted to baseband and sampled at a rate of at least twice the symbol rate of the related channel;

   an equalizer configured to equalize the data for each of the constituent channels;

   a timing recovery circuit configured to recover timing information for each of the constituent channels;

   a phase recovery circuit configured to recover phase information for each of the constituent channels; and

   an indexer that controls the cycling data through the equalizer, the timing recovery, and phase recovery circuits so that data related to each channel is processed by each of the components in sequence, thereby requiring only one phase recovery, one timing recovery and one equalization circuit for all the channels within the multi-channel band.

2. The receiver of claim 1 further comprising:

   data memory configured to store data for each of the constituent channels separately.

3. The receiver of claim 2 wherein the data memory is configured as a circular buffer.

4. The receiver of claim 3 wherein the data memory is configured as a two-way circular buffer, with data extracted from the buffer in one loop at a rate "CLK" and data written

to channel-related divisions of the buffer at rates that total the rate CLK at which data is extracted from the buffer.

5. The receiver of claim 4 wherein the rate at which data is written to each channel-related division of the buffer is equal to the rate at which data is extracted from the buffer multiplied by the ratio of storage area devoted to the channel compared to the total storage area of the data memory dedicated to storing channel data.

6. The receiver of claim 1 wherein the indexer comprises an index vector that provides an indication of which channel is related to data in each of the data memory locations dedicated to storing channel data.

7. The receiver of claim 4 wherein the rate CLK is equal to the total sampled data rate of the entire communications band.

8. The receiver of claim 1 further comprising:
a receiver front end, the front end comprising;
a down-converter configured to accept a data stream ~~data stream~~ comprising samples of the entire band sampled at a rate of at least twice the frequency of the highest frequency in the band and to convert the component channel signals within the band to baseband; and
a decimator configured to decimate a down-converted signal received from the down-converter.

9. The receiver front end of claim 8 further comprising a plurality of down-converters configured to down convert to baseband the component channels within the band in parallel.

10. The receiver front end of claim 9 further comprising a decimator configured to receive the baseband channel signals from a corresponding one of the down-converters and to decimate the corresponding baseband channel signal to a digital data stream having two samples for each symbol period of the respective channel.

11. The receiver front end of claim 10 wherein the front end is configured to down-convert and decimate a DOCSIS data stream comprising digitally modulated signals that fall within non-overlapping upstream channels that are assigned within a 5 to 42 MHz band.

12. The receiver front end of claim 10 wherein the front end is configured to down-convert and decimate a data stream in which non-overlapping channels are assigned bandwidths of approximately 3.2MHz, 1.6 MHz, .8 MHz, .4 MHz, or .2 MHz.

13. The receiver front end of claim 8 further comprising a plurality of down-converters arranged in a tree-structure to iteratively convert to baseband successively smaller portions of the frequency band.

14. The receiver front end of claim 13 wherein the down-converters are configured to iteratively convert to baseband smaller portions of the frequency band until each channel within the band is converted to baseband.

15. The receiver front end of claim 13 further comprising decimators configured to decimate the successively smaller portions of the frequency band.

16. The receiver front end of claim 15 wherein the decimators are configured to decimate each baseband channel to a sample rate that is twice the symbol rate of the baseband channel.

17. The receiver front end of claim 8 further comprising an analog to digital converter (ADC) configured to receive the full-band analog signal, to sample the entire band at greater than twice highest frequency of the band and to provide the sampled data to the down-converter.

18. A method for receiving signals in a communications system that employs digitally modulated signals operating in a band of frequencies that is divided into two or more non-overlapping channels comprising the steps of:

(A) receiving at an input a data stream representative of the entire band, with each channel within the band converted to baseband and sampled at a rate of at least twice the symbol rate of the related channel;

(B) equalizing the data for each of the constituent channels in an equalizer circuit;

(C) recovering timing information for each of the constituent channels in a timing recovery circuit;

(D) recovering phase information for each of the constituent channels in a phase recovery circuit; and

(E) indexing the cycling of data through the equalizer, the timing recovery, and phase recovery circuits so that data related to each channel is processed by each of the components in sequence, thereby requiring only one phase recovery, one timing recovery and one equalization circuit for all the channels within the multi-channel band.

19. The method of claim 18 further comprising the step of:

(F) storing data for each of the constituent channels in separate areas of data memory.

20. The method of claim 19 comprising the step of:

(F1) storing the data in data memory configured as a circular buffer.

21. The method of claim 20 comprising the step of:

(F2) storing the data in data memory configured as a two-way circular buffer whereby with data extracted from the buffer in one loop at a rate "CLK" and data is written to channel-related divisions of the buffer at rates that total the rate CLK at which data is extracted from the buffer.

22. The method of claim 21 wherein the rate at which data is written to each channel-related division of the buffer is equal to the rate at which data is extracted from the buffer multiplied by the ratio of storage area devoted to the channel compared to the total storage area of the data memory dedicated to storing channel data.

23. The method of claim 18 further comprising the step of:

(E1) the indexer providing an indication of which channel is related to data in each of the data memory locations dedicated to storing channel data.

24. The method of claim 21 wherein the rate CLK at which data is extracted from the data memory is equal to the total sampled data rate of the entire communications band.

25 The of claim 18 further comprising the steps of:

(G) down-converting and decimating digitally modulated signals operating in a band that is divided into two or more non-overlapping, with each channel occupying no more than a predetermined maximum frequency band.

26. The method of claim 25 wherein step (G) further comprises the steps of;

(G1) a down-converter accepting a data stream comprising samples of the entire band sampled at a rate of at least twice the frequency of the highest frequency in the band;

(G2) the down-converter converting the component channel signals within the band to baseband; and

(G3) a decimator decimating the down-converted signal received from the down-converter.

27. The method of claim 26 wherein the step (G2) of down-converting further comprises the step of:

(G2a) a plurality of down-converters down-converting to baseband the component channels within the band in parallel.

28. The method of claim 26 wherein the step (G3) of decimating further comprising the step of:

(G3a) a decimator receiving the baseband channel signal from a corresponding one of the down-converters decimating the corresponding baseband channel signal to a digital data stream having two samples for each symbol period of the respective channel.

29 The method of claim 26 wherein the down-converter and decimator down-convert and decimate DOCSIS compatible signals.

30. The method of claim 29 wherein the down-converter and decimator down-convert and decimate a DOCSIS data stream comprising digitally modulated signals that fall within non-overlapping upstream channels that are assigned within a 5 to 42 MHz band.

31. The method of claim 30 wherein the down-converter and decimator down-convert and decimate a data stream in which non-overlapping channels are assigned bandwidths of approximately 3.2MHz, 1.6 MHz, .8 MHz, .4 MHz, or .2 MHz.

32. The method of claim 26 wherein the step (G2) of down-converting further comprises the step of:

(G2b) a plurality of down-converters arranged in a tree-structure iteratively converting to baseband successively smaller portions of the frequency band.

33. The method of claim 32 wherein the step (G2b) further comprises the step of:

(G2c) the down-converters iteratively converting to baseband smaller portions of the frequency band until each channel within the band is converted to baseband.

34. The method of claim 26 further comprising the step of:

(G3b) decimators decimating successively smaller portions of the frequency band.

35. The method of claim 34 further comprising the step of:

(G3c) the decimators decimating each baseband channel to a sample rate that is twice the symbol rate of the baseband channel.

36. The method of claim 28 further comprising the step of:

(H) one or more analog to digital converters (ADC) receiving the full-band analog signal, the number of ADCs being fewer than the number of channels in the band,

(I) the ADCs sampling the entire band at greater than twice highest frequency of the band; and

(J) the one or more ADCs providing the sampled data to the down-converters and decimators.